

Appl. No. 10/696,151  
Amdt. dated March 21, 2005  
Reply to Office action of March 1, 2005

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (canceled)
2. (currently amended) A DRAM cell, according to claim + 10, wherein:  
the collar is disposed substantially outside of the trench.
3. (currently amended) A DRAM cell, according to claim + 10, wherein:  
the collar is disposed wholly outside of the trench
4. (currently amended) A DRAM cell, according to claim + 10, further comprising:  
~~a strap~~ the strap being disposed between the node conducting element and the cell transistor.
5. (currently amended) A DRAM cell, according to claim + 10, further comprising:  
a the strap which is being self-aligned with the collar.
6. (currently amended) A DRAM cell, according to claim + 10, further comprising:  
~~a strap~~ the strap being disposed in the trench at substantially a same depth as the collar.
7. (currently amended) A DRAM cell, according to claim + 10, further comprising:  
~~a strap~~ the strap being disposed in the trench and laterally surrounded by the collar.
8. (canceled)

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9. (canceled)

10. (currently amended) A DRAM cell comprising:

a semiconductor substrate;

a trench extending into the substrate;

a cell capacitor disposed in a bottom portion of the trench;

a cell transistor disposed in a top portion of the trench above the cell capacitor;

a node conducting element connecting the cell capacitor to the cell transistor; and

a collar disposed about the node conducting element between the cell transistor and the

cell capacitor;

wherein:

the collar is disposed in the substrate, at least partially outside of the trench, between the cell capacitor and the cell transistor;

further comprising:

a strap disposed in the trench and having an outside peripheral surface; and

the collar is laterally adjacent and surrounds the outside peripheral surface of the buried

strap;

wherein:

the strap is embedded into a top surface of the collar; and

A DRAM cell, according to claim 9, wherein:

the strap extends no higher than the collar.

11. (canceled)

12. (currently amended) A method of forming DRAM cells, comprising:

forming trenches in extending into a semiconductor substrate;

forming cell capacitors in a bottom portions of the trenches;

forming cell transistors in a top portions of the trenches above the cell capacitors; and

for each DRAM cell, providing a node conducting element between the cell capacitor and

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the cell transistor;

for each DRAM cell, providing a collar disposed about the node conducting element  
between the cell capacitor and the cell transistor, ~~the collar being disposed in the substrate, at~~  
~~least partially outside of the trench;~~

for each DRAM cell, forming a recess in a top inside corner of the collar, and

for each DRAM cell, embedding a strap in the recess[[]];

wherein the strap extends no higher than the collar.

13. (previously presented) A method, according to claim 12, wherein:  
the collar is disposed at least substantially outside of the trench.
14. (previously presented) A method, according to claim 12, wherein:  
the collar is disposed wholly outside of the trench.
15. (canceled)
16. (canceled)
17. (canceled)
18. (canceled)
19. (currently amended) A method, according to claim 12, ~~further comprising:~~  
~~for each DRAM cell, disposing [[a]] strap in the trench at substantially a same depth as~~  
~~the collar;~~  
~~wherein the strap extends no higher than the collar.~~  
wherein the collar is disposed in the substrate, at least partially outside of the trench,
20. (currently amended) A method, according to claim 12, further comprising:

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for each DRAM cell, disposing a the strap in the trench; and  
the strap is laterally surrounded by the collar.

21. (currently amended) A DRAM cell, according to claim ~~1~~ 10, further comprising:  
a recess disposed in a top inside corner of the collar; and  
the strap extends into the recess in the top inside corner of the collar.
22. (currently amended) A DRAM cell comprising:  
a semiconductor substrate;  
a trench extending into the substrate;  
a cell capacitor disposed in a bottom portion of the trench;  
a cell transistor disposed in a top portion of the trench above the cell capacitor;  
a node conducting element connecting the cell capacitor to the cell transistor; and  
a collar disposed about the node conducting element between the cell transistor and the  
cell capacitor;  
wherein:  
the collar is disposed in the substrate, at least partially outside of the trench, between the  
cell capacitor and the cell transistor;  
further comprising:  
a strap disposed in the trench and having an outside peripheral surface; and  
the collar is laterally adjacent and surrounds the outside peripheral surface of the buried  
strap;  
~~A DRAM cell, according to claim 1, wherein:~~  
the strap is fully vertically embedded in the collar and it is laterally surrounded by the  
collar.
23. (currently amended) A DRAM cell, according to claim ~~1~~ 22, wherein:  
the strap is disposed in the trench at substantially a same depth as the collar; and  
the collar extends deeper into the trench than the strap and ~~and~~ covers a bottom surface of

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the strap.

24. (currently amended) A DRAM cell, according to claim ~~1~~ 22, wherein:  
the collar covers a bottom surface of the strap.
25. (original) A method, according to claim 12, wherein:  
constraining outward diffusion of the strap by the laterally-surrounding collar; and  
constraining downward diffusion of the strap with the collar.
26. (original) A method, according to claim 12, wherein:  
an upper surface of the buried strap does not extend above an upper surface of the collar.

Please enter the following:

27. (new) A method, according to claim 12, wherein:  
the collar covers a bottom portion of the strap.
28. (new) A method, according to claim 12, wherein:  
the strap is fully vertically embedded in the collar and it is laterally surrounded by the  
collar.